AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method comprising:

maintaining a first page table map for use in an isolated execution mode and a second page table map for use in a normal execution mode;

dynamically swapping between the first page table map and the second page table map responsive to a change in execution mode;

identifying if an event is one of a class of events to be handled in the isolated execution mode; and

handling the event using the first page table map if the event is identified as one of the class of events to be handled ~~by~~ in the isolated execution mode.

2. (Currently Amended) The method of claim 1 further comprising:

identifying if the event is one of a class of events to be handled in the isolated execution mode; and

handling the event using the first page table map if the event is identified as one of the class of events to be handled ~~by~~ in the isolated execution mode~~.~~;

wherein identifying comprises indexing into a lookup table with a exception vector of the event.

3. (Original) The method of claim 1 wherein dynamically swapping comprises:

loading a set of control registers selected based on an exception vector of the event.

4. (Original) The method of claim 3 wherein the set of control registers comprises:

a global descriptor table register;

an interrupt descriptor table register; and

a page table map base address register.

5. (Original) The method of claim 1 wherein maintaining comprises:

mirroring a page table base address register.

6. (Original) The method of claim 1 further comprising:

defining a set of events that should be handled in isolated execution mode.

7. (Original) The method of claim 6 wherein the set of events to be handled in the isolated execution mode comprises:

machine check events and clock events.

8. (Currently Amended) The method of claim ~~21~~ 1 wherein handling comprises:

determining if a current mode is the isolated execution mode;

loading a set of control registers with values corresponding to the first page table map if the current mode is not the isolated execution mode and the event is one of the class; and

dispatching an exception vector after the loading is complete.

9. (Original) An apparatus comprising:

a first storage location storing control data for a first page table map;

a second storage location storing control data for a second page table map; and

a selection unit to select which page table map is applied responsive to receipt of an event.

10. (Original) The apparatus of claim 9 wherein the selection unit comprises:

a multiplexer that selects between the first and the second storage locations based on an exception vector of the event.

11. (Original) The apparatus of claim 9 wherein the first storage location contains a base address for the first page table map and the second storage location contains a base address for the second page table map.

12. (Currently Amended) A platform comprising:

a processor executing in one of normal execution mode and isolated execution mode;

a first set of control registers to define a current memory map of the platform; and

a mapping unit to dynamically load the first set of control registers responsive to an event~~,~~ if the event should be handled using an alternate memory map.

13. (Original) The platform of claim 12 wherein the mapping unit comprises:

a second set of registers having a first subset corresponding to control register values for a normal execution mode memory map and a second subset corresponding to control register values for an isolated execution mode memory map; and

a selection unit to select between the first subset and the second subset.

14. (Original) The platform of claim 13 wherein the selection unit comprises:

a plurality of multiplexers having selection driven by an exception vector of an incoming event.

15. (Original) The platform of claim 12 wherein the first set of control registers comprises:

a global descriptor table register;

an interrupt description table register; and

a page table map base address register.

16. (New) A method comprising:

distinguishing between at least two execution modes of a central processing unit in an information processing system;

maintaining at least two sets of processor control registers within the central processing unit;

recognizing an asynchronous event;

determining which execution mode is desired for responding to the asynchronous event; and

if the current execution mode is not the same as the desired execution mode for responding to the asynchronous event, altering the current execution mode to the desired execution mode before responding to the asynchronous event, wherein

at least one set of processor control registers is inaccessible to the processor in at least one of the execution modes.

17. (New) The method of Claim 16 wherein the at least two sets of processor control registers comprise virtual memory management registers.

18. (New) The method of Claim 16 wherein the at least two sets of processor control registers comprise interrupt vector table registers.

19. (New) The method of Claim 16 wherein the asynchronous event is a machine check event.

20. (New) The method of Claim 16 wherein the asynchronous event is a clock interrupt.

21. (New) The method of Claim 16 wherein the asynchronous event is a hardware interrupt.

22. (New) An apparatus comprising:

a central processing unit (CPU) capable of operating in one of at least two execution modes;

a storage location that identifies a current execution mode of the CPU;

a plurality of resources operatively joined to the CPU; and

a mechanism to restrict access to a subset of the plurality of resources based on the current execution mode of the CPU.

23. (New) The apparatus of Claim 22 wherein the mechanism to restrict access to a subset of the plurality of resources comprises a signal provided by the CPU that indicates whether the current execution mode permits access to the plurality of resources.

24. (New) The apparatus of Claim 22 wherein the resource to which access is restricted is a special-purpose control register.

25. (New) The apparatus of Claim 24 wherein the special purpose control register is a virtual memory management descriptor.

26. (New) The apparatus of Claim 24 wherein the special purpose control register is an interrupt vector table descriptor.

27. (New) The apparatus of Claim 22 wherein the resource to which access is restricted is a device located outside the CPU.

28. (New) The apparatus of Claim 22 wherein the resource to which access is restricted is a random-access memory location.

29. (New) A method of preventing inadvertent disclosure of information contained within a CPU comprising:

distinguishing between a normal and an isolated execution mode;

maintaining a separate set of control registers that are only accessible when the CPU is operating in the isolated execution mode;

defining a set of events that should be handled in the isolated execution mode;

determining if an event is a member of the set of events when the event occurs; and

if the event is a member of the set of events and the CPU is operating in the normal execution mode, switching to the isolated execution mode before executing instructions in response to said event.

30. (New) The method of Claim 29 wherein the set of events comprises machine check exceptions and clock events.